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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,775	10/30/2003	Masayuki Furuhashi	032076	7971

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EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,775	FURUHASHI ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-7,20,22 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-19, 21, 23, 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 16 September 2005.

Election/Restrictions

1. Claims 1-7, 20, 22, 24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 21 March 2005.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 8, 16-17, 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Moore (US 2002/0111039 A1).

Referring to paragraphs [0022] to [0031], Moore teaches a method for depositing a silicon oxynitride film (i.e. SiON). The deposition temperature is desirably in the range of 500 to 650 degrees C (see paragraph [0023]). In one embodiment, carbon is incorporated into the oxynitride film (i.e. SiOCN is formed – see paragraph [0028]). The process gases used to deposit the SiOCN film include bistertiarybutylaminosilane (BTBAS) as a silicon source compound (also a nitrogen containing compound because the amino component implies a derivative from ammonia), along with a particularly preferred combination of ammonia (NH_3), nitrous oxide (N_2O), and nitric oxide (NO) as nitrogen source compounds (see paragraphs [0024] and [0025]).

These are all of the limitations set forth in claims 8, 16-17, 19 of the applicant's invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8-11, 15, 17-19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arghavani et al. (US 2004/0033677 A1) in view of Luo et al. (US 2003/0059535 A1).

Referring to Figs. 3A to 3M and paragraphs [0013] to [0038], Arghavani et al. disclose a method for forming a field effect transistor that includes the following features:

- A gate dielectric (319) formed on a semiconductor substrate (300) and underneath a gate electrode (318) as shown in Fig. 3I;
- Shallow source/drain extension regions (340) implanted into the top substrate surface as shown in Fig. 3J;
- Silicon oxide layer (341) and silicon nitride layer (342) sequentially deposited over the gate structure as shown in Fig. 3K;
- The silicon nitride layer (342) can be formed by thermal CVD at a substrate temperature between 500 and 650 degrees C using bistertiarybutylaminosilane (BTBAS) precursor, molecular nitrogen (N_2), and ammonia (NH_3) process gases as described in paragraph [0026];
- The silicon nitride layer (342) and silicon oxide layer (341) are then anisotropically etched to form spacers (344) as shown in Fig. 3L; and
- Deep source/drain regions (348) are then implanted in a self-aligned manner as shown in Fig. 3M.

These are limitations set forth in claims 8-11, 15, 17, 19, 21 of the applicant's invention.

However, Arghavani et al. do not teach or suggest a compound containing a plurality of nitrogen in a molecule excepting N_2, which is a limitation of claim 8. More particularly, Arghavani et al. do not teach or suggest that this compound is a hydrazine compound or an azido compound, which is the further limitation to claim 8 as set forth in claim 18 of the applicant's invention.

Luo et al. teach that hydrazine can be used as an alternative nitrogen source to ammonia for depositing silicon nitride layers (see paragraphs [0051] and [0052]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the CVD method of Arghavani et al. for depositing the silicon nitride layer by substituting hydrazine for ammonia as taught by Luo et al. Luo et al. recognize that hydrazine is an alternative to ammonia as a nitrogen source for depositing silicon nitride layers (see paragraph [0052]).

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arghavani et al. (US 2004/0033677 A1) and Luo et al. (US 2003/0059535 A1) as applied to claim 11 above, and further in view of Moore (US 2002/0111039 A1).

As shown above, the combination of Arghavani et al. and Luo et al. has all of the limitations as set forth in claim 11 of the applicant's invention. However, this combination lacks the further limitations to claim 11 as set forth in claim 12, which are directed to burying an interconnect in a further another insulation film. Moore teaches the formation of a BPSG insulator layer (120) over a substrate (112) that includes gate stacks (116) with spacers (117), selectively etching a contact opening (124) through the

BPSG layer (120) with respect to the spacers (117), and providing a conductive plug (130) in the contact opening (124) (see Fig. 4 and paragraph [0034])).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Arghavani et al., Luo et al., and Moore in order to form conductive plugs through an insulating layer, as taught by Moore, for making electrical connections to the source/drain regions of Arghavani et al. Moore recognizes that by selectively etching their BPSG layer with respect to the spacer material, electrical shorting between the conductive plugs and the gate electrodes will be avoided (see paragraph [0034]).

7. Claim 8, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xia et al. (US 6,153,261) in view of Luo et al. (US 2003/0059535 A1).

Referring to column 10, lines 44-67, Xia et al. teach a thermal CVD method for depositing a silicon nitride film (i.e. SiN) using a substrate temperature that is set at a temperature in the range of 500 to 650 degrees C. The process gases used to deposit the SiN film include bistertiarybutylaminosilane (BTBAS) precursor, molecular nitrogen (N_2), and ammonia (NH_3). These are limitations as set forth in claims 8, 17, 19 of the applicant's invention.

However, Xia et al. do not teach or suggest a compound containing a plurality of nitrogen in a molecule excepting N_2, which is a limitation of claim 8. More particularly, Xia et al. do not teach or suggest that this compound is a hydrazine compound or an

azido compound, which is the further limitation to claim 8 as set forth in claim 18 of the applicant's invention.

Luo et al. teach that hydrazine can be used as an alternative nitrogen source to ammonia for depositing silicon nitride layers (see paragraphs [0051] and [0052]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the CVD method of Xia et al. by substituting hydrazine for ammonia as taught by Luo et al. Luo et al. recognize that hydrazine is an alternative to ammonia as a nitrogen source for depositing silicon nitride layers (see paragraph [0052]).

8. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xia et al. (US 6,153,261) and Luo et al. (US 2003/0059535 A1) as applied to claim 8 above, and further in view of Huang et al. (US 6,077,769).

As shown above, the combination of Xia et al. and Luo et al. has all of the limitations as set forth in claim 8 of the applicant's invention. However, this combination lacks the further limitations to claim 8 as set forth in claims 13-14, which are directed to forming an interconnect in a further another insulation film. Referring to Figs. 2A-2G and column 3, line 14 to column 4, line 49, Huang et al. teach a method of forming an interconnect over a substrate with MOS transistors (not shown) located on the substrate. IMD layers (114, 124) that can be silicon dioxide (i.e. an another insulation film and a further another insulation film) and a hard mask layer (126) that can be silicon nitride (i.e. an insulation film) are sequentially formed over the substrate (100) as shown

in Fig. 2A. Interconnect holes (125, 135a) are then formed in the IMD layer (124) and the hard mask layer (126) as shown in Fig. 2E. The interconnect holes are than filled with a metal layer (130), which includes polishing back the excess metal by CMP to the hard mask layer (126) as shown in Fig. 2F. Regarding claim 14, the same method can be used to form additional interconnect levels (see column 4, lines 38-39), in which case the insulation film can correspond to a hard mask layer that overlies the interconnect (130) of Fig. 2F.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Xia et al., Luo et al., and Huang et al. in order to form the hard mask layer of Huang et al. by using the silicon nitride CVD method as taught by Xia et al. and Luo et al. Xia et al. recognize that the use of BTBAS as the silicon source for their CVD method has the advantage of an increased deposition rate (see column 2, lines 29-41).

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arghavani et al. (US 2004/0033677 A1) and Luo et al. (US 2003/0059535 A1) as applied to claim 9 above, and further in view of Lee et al. (US 2002/0151145 A1).

As shown above, the combination of Arghavani et al. and Luo et al. has all of the limitations as set forth in claim 9 of the applicant's invention. However, this combination lacks the further limitations to claim 9 as set forth in claim 23, which are directed to using another sidewall spacer as a mask for implanting deeper dopant diffused regions and subsequently removing the mask by etching. Referring to Figs. 1-6 and paragraphs

[0011] to [0022], Lee et al. disclose a CMOS fabrication method that includes using sacrificial spacers (22a, 22b) as a mask for implanting deep source/drain regions (24a, 24b), removing the sacrificial spacers by etching, then implanting shallow source/drain extension regions (26a, 26b) as well as halo regions (28a, 28b), and then forming final sidewall spacers (30a, 30b).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Arghavani et al., Luo et al., and Lee et al. in order to use sacrificial spacers to form the deep implants first, as taught by Lee et al., in the transistors of Arghavani et al. Lee et al. recognize that the deep implants can be annealed prior to forming the halo regions and thereby minimizes diffusion of halo dopants from the subsequently formed halo regions (see paragraph [0028]).

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arghavani et al. (US 2004/0033677 A1) and Luo et al. (US 2003/0059535 A1) as applied to claim 9 above, and further in view of Chatterjee (US 2003/0102512 A1).

As shown above, the combination of Arghavani et al. and Luo et al. has all of the limitations as set forth in claim 9 of the applicant's invention. However, this combination lacks the further limitations to claim 9 as set forth in claim 25, which are directed to forming pocket regions. Chatterjee teaches a pMOS device (12) with n-type pocket regions (31) formed adjacent to p-type source/drain extensions as shown in Fig. 1,

which implies that the pocket regions (31) are formed prior to the formation of sidewall insulators on the pMOS gate stack (34) (also see paragraph [0019]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Arghavani et al., Luo et al., and Chatterjee in order to form pocket regions, as taught by Chatterjee, in the transistors of Arghavani et al. Chatterjee recognizes that pocket implants effectively reduce the sensitivity of the threshold voltage to the channel length of a field effect transistor (see paragraph [0019]).

Response to Arguments

11. Regarding the combination of Xia et al. and Luo et al., the applicant's arguments filed 16 September 2005 (see pages 16-17) have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

As indicated above, the combined teachings of Xia et al. and Luo et al. suggest that hydrazine can be substituted for ammonia, in which case a silicon nitride film would

be deposited using BTBAS, nitrogen, and hydrazine as source gases. The fact that the applicant has designated their source gases in the claims as "a first raw material", "a second raw material", "a third raw material", etc., has no patentable weight. In other words, BTBAS can be "a first raw material" and hydrazine can be "a second raw material". It is agreed that claim 16 requires that ammonia be used as a raw material. However, none of the rejected claims, based on the combination of Xia et al. and Luo et al., depend on claim 16 and, accordingly, do not require the use of ammonia as a raw material.

12. Applicant's remaining arguments with respect to claims 8-17, 19, 21, 23, 25 have been considered but are moot in view of the new grounds of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mizuno et al. teach a CVD method for forming silicon oxynitride that utilize BTBAS, NH_3, and N_2O as raw gases.

14. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER